What is claimed is:

1. A thin film transistor, comprising:

a substrate;

a crystallized semiconductor layer formed over the substrate having a channel region, low-density impurity regions and high-density impurity regions;

a gate insulating layer formed on the crystallized semiconductor layer;

a first gate electrode formed on the gate insulating layer having a width corresponding to the channel region;

a second gate electrode formed on the first gate electrode and on the gate insulating layer such that the second gate electrode overlaps the low-density impurity regions; and

a source electrode and a drain electrode respectively contacting the high-density impurity regions.

2. The thin film transistor of claim 1, wherein the crystallized semiconductor layer is a polycrystalline silicon layer.

3. The thin film transistor of claim 1, wherein the low-density impurity regions are n^- regions.

4. The thin film transistor of claim 1, wherein the high-density impurity regions are n+ regions.

5. The thin film transistor of claim 1, wherein the first gate electrode and the second gate electrode are made of the same materials.

6. The thin film transistor of claim 1, further comprising:

a buffer layer formed on the substrate.

7. The thin film transistor of claim 1, further comprising:

an insulating layer formed over the second gate electrode, wherein the source electrode and the drain electrode are contacted to the high-density impurity regions through respective contact holes in the insulating layer.

8. The thin film transistor of claim 1, wherein the second gate electrode layer has a width greater than a width of the first gate electrode layer.

9. The thin film transistor of claim 1, wherein the channel region has a width corresponding to the width of the first gate electrode layer.

10. A liquid crystal display device, comprising:

a first substrate and a second substrate;

a plurality of gate lines and data lines formed over the first substrate so as to define a plurality of pixels;

thin film transistors arranged in the plurality of pixels that each include a polycrystalline semiconductor layer including a channel region between low-density impurity regions that are in between high-density impurity regions, a gate insulating layer formed on the polycrystalline semiconductor layer, a first gate electrode formed on the gate insulating layer corresponding to the channel region, a second gate electrode formed on the first gate electrode and on the gate insulating layer such that the second gate electrode overlaps the low-density impurity regions, and a source electrode and a drain electrode contacted to the high-density impurity regions;

a pixel electrode formed in the pixel area;

a color filter layer formed on the second substrate; and

a liquid crystal layer formed between the first substrate and the second substrate.

11. The liquid crystal display device of claim 10, wherein the first gate electrode and the second gate electrode are made of different materials.

12. A liquid crystal display device, comprising:

a first substrate including a pixel area and a driving circuit area;

a first thin film transistor formed in the pixel area;

a second thin film transistor formed in the driving circuit area, the second thin film transistor including two layers of gate electrodes, a semiconductor layer having a low-density impurity regions overlapped with only one of the gate electrode layers, a source electrode and a drain electrode; and

a third thin film transistor formed in the driving circuit area.

13. The liquid crystal display device of claim 12, wherein the low-density impurity regions are n^- regions.

14. The liquid crystal display device of claim 12, wherein the third thin film transistor is a p-type thin film transistor.

15. The liquid crystal display device of claim 12, wherein the first thin film transistor is a gate overlapped lightly doped drain thin film transistor.

16. The liquid crystal display device of claim 15, wherein the first thin film transistor includes:

two layers of gate electrodes formed over the substrate;

a polycrystalline semiconductor layer arranged under the gate electrodes such that at least a part of lightly doped drain regions is overlapped by only one layer of the gate electrodes; and

a source electrode and a drain electrode.

17. The liquid crystal display device of claim 12, wherein the first thin film transistor is a lightly doped drain thin film transistor.

18. The liquid crystal display device of claim 17, wherein the first thin film

transistor includes:

a polycrystalline semiconductor layer having a channel region between low-density impurity regions that are in between high-density impurity regions;

a gate electrode arranged over the channel region; and

a source electrode and a drain electrode.

19. The liquid crystal display device of claim 12, wherein the first thin film transistor is a p-type thin film transistor.

20. The liquid crystal display device of claim 12, further comprising:

a second substrate on which a color filter layer is formed; and

a liquid crystal layer formed between the first substrate and the second substrate.

21. The thin film transistor of claim 12, wherein a first layer and a second layer of the two layers of gate electrodes are made of different materials.

22. A method for fabricating a thin film transistor, comprising:

providing a substrate;

forming a polycrystalline semiconductor layer over the substrate;

forming a gate insulating on the polycrystalline semiconductor layer;

forming a first gate electrode on the gate insulating layer using a mask;

forming a low-density impurity regions by introducing low-density impurities into the

polycrystalline semiconductor layer after blocking the polycrystalline semiconductor layer with the first gate electrode;

forming a second gate electrode having a width greater than that of the first gate electrode;

forming a high-density impurity regions by introducing high-density impurities into portions of the low-density impurity regions after blocking parts of the low-density impurity regions with the second gate electrode; and

forming a source electrode and a drain electrode respectively contacted to the high-density impurity regions.

23. The method of claim 22, wherein forming the polycrystalline semiconductor layer includes the sub-steps of:

forming a polycrystalline silicon layer; and

etching the polycrystalline silicon layer.

24. The method of claim 22, wherein forming the polycrystalline semiconductor layer includes the sub-steps of:

forming an amorphous semiconductor layer;

crystallizing the amorphous semiconductor layer into a polycrystalline semiconductor layer by applying heat; and

etching the polycrystalline semiconductor layer.

25. The method of claim 22, wherein forming the polycrystalline semiconductor layer includes the sub-steps of:

forming an amorphous semiconductor layer;

crystallizing the amorphous semiconductor layer into a polycrystalline semiconductor layer by irradiating laser; and

etching the polycrystalline semiconductor layer.

26. The method of claim 22, wherein forming the first gate electrode includes the sub-steps of:

forming a first metal layer on the gate insulating layer;

forming a photoresist pattern on the first metal layer using a mask; and

over-etching the first metal layer.

27. The method of claim 26, wherein the over-etching is isotropic-etching.

28. The method of claim 22, wherein forming the first gate includes the sub-steps of:

forming a first metal layer on the gate insulating layer;

forming a photoresist pattern on the first metal layer using the mask;

ashing the photoresist pattern; and

etching the first metal layer using the ashed photoresist pattern as a mask.

29. The method of claim 22, wherein forming the second gate electrode includes the sub-steps of:

forming a second metal layer on the gate insulating layer;

forming a photoresist pattern on the second metal layer using said mask; and

etching the second metal layer.

30. The method of claim 22, wherein forming second gate electrode includes the sub-steps of:

positioning the first gate electrode and an opposed electrode into an electrolyte; and

electroplating a metal layer onto the first gate electrode by applying a voltage.

31. The method of claim 22, wherein the first gate electrode and the second electrode are made of different materials.

32. The method of claim 22, wherein the low-density impurities are n^- ions and the high-density impurities are n^+ ions.

33. The method of claim 22, further comprising:

forming a buffer layer on the substrate.

34. The method of claim 22, further comprising:

forming an insulating layer on the second gate electrode; and

forming a contact hole in the insulating layer to contact the drain electrode to one of the high-density impurity regions.

35. A method for fabricating a thin film transistor, comprising:

providing a substrate over which a polycrystalline semiconductor layer is formed;

forming a gate insulating layer on the polycrystalline semiconductor layer;

forming a first gate electrode on the gate insulating layer;

introducing low-density impurities into the semiconductor layer using the first gate electrode as a mask;

forming a second gate electrode having a width greater than that of the first gate electrode;

introducing high-density impurities into the semiconductor layer using the second gate electrode as a mask; and

forming a source electrode and a drain electrode.

36. The method of claim 35, wherein the first gate electrode and the second gate electrode are formed using the same mask.

37. The method of claim 36, wherein forming the first gate electrode includes the sub-steps of:

forming a first metal layer;

forming a photoresist pattern using the mask; and

over-etching the first metal layer.

38. The method of claim 36, wherein forming the first gate electrode includes the sub-steps of:

forming a first metal layer;

forming a photoresist pattern using the mask;

reducing a width of the photoresist pattern by ashing it; and

etching the first metal layer.

39. The method of claim 35, wherein the first gate electrode is formed by photolithography process and the second gate electrode is formed by electroplating method.

40. A method for fabricating a liquid crystal device, comprising:

providing a first substrate and a second substrate;

forming a polycrystalline semiconductor layer over the first substrate;

forming a gate insulating layer on the polycrystalline semiconductor layer;

forming a first gate electrode on the gate insulating layer using a mask;

forming low-density impurity regions by introducing low-density impurities into the polycrystalline semiconductor layer after blocking the polycrystalline semiconductor layer with the first gate electrode;

forming a second gate electrode having a width greater than that of the first gate electrode using the mask;

forming a high-density impurity regions by introducing high-density impurities into portions of the low-density impurity regions after blocking parts of the low-density impurity regions with the second gate electrode;

forming a source electrode and a drain electrode respectively contacted to the high-density impurity regions;

forming a passivation layer over the whole surface of the first substrate;

forming a pixel electrode on the passivation layer;

forming a color filter layer on the second substrate; and

forming a liquid crystal layer between the first and second substrates.

41. The method of claim 40, wherein the first gate electrode and the second electrode are made of different materials.

42. A method of fabricating a liquid crystal display panel, comprising:

providing a first substrate divided into a pixel area and a driving circuit area;

forming a first thin film transistor in the driving circuit area having a first semiconductor layer, wherein the first thin film transistor has two layers of gate electrodes in which only one of the layers overlaps low-density impurity regions in the first semiconductor layer;

forming a second thin film transistor in the driving circuit area; and

forming a third thin film transistor in the pixel area.

43. The method of claim 42, wherein forming the first thin film transistor includes the sub-steps of:

forming the first semiconductor layer as a first crystallized semiconductor layer;

forming a gate insulating on the first crystallized semiconductor layer;

forming a first gate electrode on the gate insulating layer;

forming first low-density impurity regions by introducing low-density impurities;

forming a second gate electrode having a width greater than that of the first gate electrode;

introducing high-density impurities into the first low-density impurity regions by using the second gate electrode as a mask; and

forming a first source electrode and a first drain electrode.

44. The method of claim 43, wherein the first gate electrode is formed using a photolithography process and the second gate electrode is formed using an electroplating method.

45. The method of claim 43, wherein forming the second thin film transistor includes the sub-steps of:

forming a second crystallized semiconductor layer;

forming a third gate electrode on the second crystallized semiconductor layer;

introducing impurities into the second crystallized semiconductor layer using the third gate electrode as a mask; and

forming a second source electrode and a second drain electrode.

46. The method of claim 43, wherein forming the third thin film transistor includes the sub-steps of:

forming a third crystallized semiconductor layer;

forming a gate insulating on the third crystallized semiconductor layer;

forming a fourth gate electrode on the gate insulating layer;

forming second low-density impurity regions by introducing low-density impurities into the third crystallized semiconductor layer using the fourth gate electrode as a mask;

forming a fifth gate electrode having a width greater than that of the fourth gate electrode;

introducing high-density impurities into portions of the second low-density impurity regions using the fifth gate electrode as a mask; and

forming a third source electrode and a third drain electrode.

47. The method of claim 43, wherein forming the third thin film transistor includes the sub-steps of:

forming a third crystallized semiconductor layer;

forming a gate insulating on the third crystallized semiconductor layer;

forming a fourth gate electrode on the gate insulating layer;

forming a second low-density impurity regions by injecting low-density impurities into the third crystallized semiconductor layer using the fourth gate electrode as a mask;

introducing high-density impurities into portions of second low-density impurity

regions; and

forming a third source electrode and a third drain electrode.

48. The method of claim 47, wherein introducing high-density impurities into portions of second low-density impurity regions is done after blocking a region including the gate electrode.

49. The method of claim 43, wherein forming the third thin film transistor includes:

forming a third semiconductor layer;

forming a fourth gate electrode over the third semiconductor layer;

introducing impurity into the third semiconductor layer using the fourth gate electrode as a mask; and

forming a second source electrode and a second drain electrode.

50. The method of claim 43, wherein gates of the first, second and third thin film transistors are formed using the same mask.